

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
30 January 2003 (30.01.2003)

PCT

(10) International Publication Number  
**WO 03/009414 A1**

(51) International Patent Classification<sup>7</sup>: **H01P 5/18**

(21) International Application Number: **PCT/US02/23045**

(22) International Filing Date: **18 July 2002 (18.07.2002)**

(25) Filing Language: **English**

(26) Publication Language: **English**

(30) Priority Data:  
**09/910,311 19 July 2001 (19.07.2001) US**

(71) Applicant: **CREE MICROWAVE, INC. [US/US]; 160 Gibraltar Court, Sunnyvale, CA 94089 (US).**

(72) Inventor: **CRESCENZI, Emil, James, Jr.; 640 Ashby Lane, Cambria, CA 93428-0277 (US).**

(74) Agents: **WOODWARD, Henry, K. et al.; Townsend and Townsend and Crew LLP, Two Embarcadero Road, 8th Floor, San Francisco, CA 94111-3834 (US).**

(81) Designated States (national): **AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,**

**CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.**

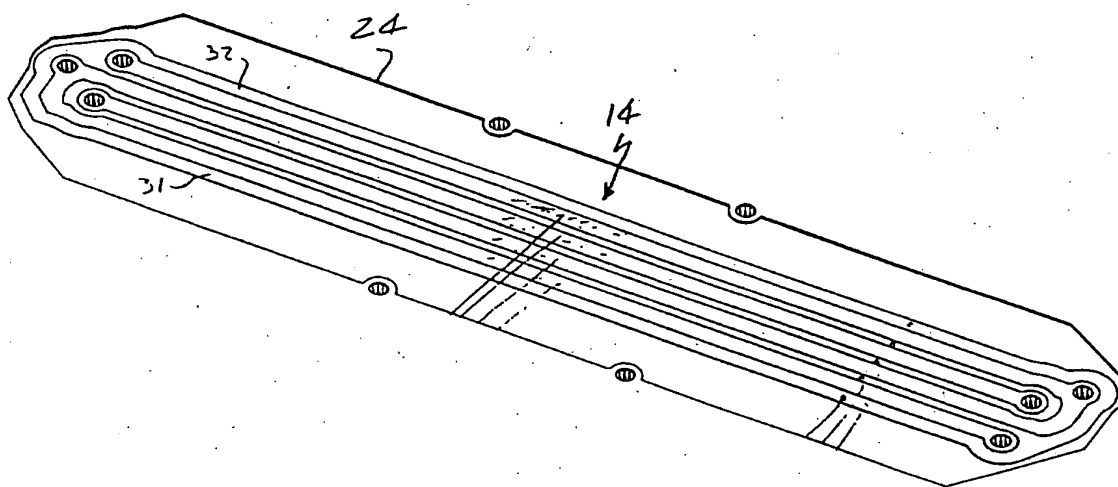
(84) Designated States (regional): **ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).**

**Published:**

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: **INVERTED COPLANAR WAVEGUIDE COUPLER WITH INTEGRAL MICROSTRIP CONNECTION PORTS**



(57) Abstract: A coplanar coupler (14) for use with microstrip input and output ports includes a printed circuit substrate in which first and second metal input ports are formed on a top surface and cooperate with a metal layer on the bottom surface as microstrip lines, and a first and second metal output ports formed on the top surface which cooperate with the metal layer on the bottom surface as microstrip lines. The metal layer (24) on the bottom surface functions as a ground plane for the input ports and output ports, the metal layer being removed in a coupler region underlying at least portions of the metal input and output ports and extending therebetween. First and second metal lines (31, 32) are formed on the bottom surface in the coupler region and function as a coplanar coupler for the input and output ports. Electrical vias in the substrate interconnect the ports and the coplanar coupler.

**WO 03/009414 A1**

## INVERTED COPLANAR WAVEGUIDE COUPLER WITH INTEGRAL MICROSTRIP CONNECTION PORTS

### BACKGROUND OF THE INVENTION

5           This invention relates generally to microwave circuits, and more particularly the invention relates to signal couplers as used in microwave circuits. Microwave circuits often use signal couplers between circuit sections. Numerous coupling structures have been used in the past, including microstrip coupled lines, stripline coupled lines, and coplanar waveguide coupled lines. The most common form of microwave circuitry is microstrip transmission lines. Microstrip couplers, such as the Lange coupler, are difficult to  
10       manufacture in printed circuit boards which have limited and rather coarse resolution of lines and spaces. This is particularly true when one requires high coupling values on the order of -3 dB (i.e., one-half of the incident energy). It has been demonstrated previously that a coplanar waveguide coupler can satisfy the high value coupling while only requiring medium  
15       resolution of line widths and gaps. However, a coupler realized entirely in coplanar waveguide form requires microstrip-to-coplanar waveguide transitions which consume space and place restrictions on circuit design.

          Frick U.S. Patent No. 5,629,654 discloses a totally coplanar waveguide construction. However, for many applications it is desirable to have microstrip transmission  
20       line input and output ports. Prior art designs require separate microstrip-to-coplanar transitions in order to use a coplanar waveguide coupler with microstrip input and output ports. This adds complexity to circuit design and consumes additional circuit board space.

          The present invention is directed to providing a coplanar coupler for microstrip input/output ports which is space efficient and compatible with printed circuit  
25       board manufacturing considerations while providing requisite coupling value, terminal return loss, and isolation.

### BRIEF SUMMARY OF THE INVENTION

          In accordance with the invention, a planar coupler for microstrip input and output ports in a microwave circuit is fabricated on a printed circuit substrate in which the  
30       microstrip input and output lines are on one surface of the substrate, and the coplanar coupler

lines are on an opposite surface of the substrate with vias interconnecting the microstrip ports with the coplanar coupler lines.

A metal layer is formed on the surface with the coplanar coupler, but is spaced from the coupler. The metal layer functions with the input and output ports in forming the microstrip ground plane.

In a preferred embodiment, first and second metal lines of the coplanar coupler are in spaced parallel alignment, and preferably comprise U-shaped metal traces. A bias metal line can be placed on the surface with the input and output ports which extends across and spaced from the coplanar coupler lines on the opposing surface for providing bias voltage to circuit components mounted on the surface. By grounding the bias metal line, the coplanar coupler can include a partial grounded coplanar waveguide. The amount of the grounded coplanar waveguide center region can be adjusted to optimize the characteristics of the overall coupler.

The structure in accordance with the invention is efficient in substrate space which results in cost, manufacturing, and application enhancements. The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a functional block diagram of a quadrature balanced amplifier module in which couplers in accordance with the invention can be employed.

Fig. 2 is a top view illustrating metal traces on top and bottom surfaces of a printed circuit substrate for a coplanar coupler in accordance with one embodiment of the invention.

Fig. 3A is a plan view of metalization for the input and output ports on one surface of the structure of Fig. 2, and Fig. 3B is a plan view of metalization for the coplanar coupler on the bottom surface of the structure of Fig. 2.

Fig. 4 is a three dimensional view of the metal traces on the top and bottom surfaces and the interconnecting vias.

#### DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Fig. 1 is a functional block diagram of a microwave circuit in which an input signal at 10 is applied through a coupler 12 to quadrature balance amplifiers 54, 56 with the amplified outputs of the amplifiers applied through coupler 18 to an output 20. Typically, the

input line 10 and output line 20 are microstrip comprising a metal trace on one surface of a substrate over a grounded metal layer on the opposing surface of the substrate, and couplers 12, 18 are coplanar metal traces. Frick U.S. Patent No. 5,629,654 discloses input and output microstrip with coplanar coupler 12 all formed on one surface of the printed circuit of the substrate. As noted above, this arrangement is not cost or space effective.

In accordance with the present invention, improved cost and performance are realized by placing the microstrip input and output lines on one surface of the substrate and placing the coplanar coupler lines on another surface of the substrate with the input and output lines connected to the coplanar coupler by feedthrough vias through the substrate. The substrate can be ceramic with gold, silver, or copper metal lines, or other suitable substrates and metal layers can be used. Fig. 2 is a plan view of the circuitry of Fig. 1 realized using a coplanar coupler in accordance with the present invention. In this view, all metal traces and circuitry are on the top surface of the substrate except for the couplers 14 and 16 which are on the bottom surface. Input port 10 and isolation port 11 comprise metalization on the top surface which cooperates with a metalized layer on the bottom surface to form a microstrip input line. Similarly, output port 20 and an isolation port 21 comprise metalization on the top surface which cooperates with the metalization on the bottom surface as a microstrip output line. The coplanar couplers 14, 16 comprise metalization on the bottom surface formed in areas 24, 26 where the backside metalization has been removed. Planar coupler 14 comprises interdigitated U-shaped metal traces 31, 32 with metal trace 31 connected by throughhole vias 33 to input metalization 10 and to metal trace 34 through via 35. Similarly, U-shaped metal trace 32 is connected to isolation port 11 through vias 36 and to microstrip trace 38 through via 39. Closely spaced parallel lines 31 and 32 form the coupled lines. Microstrip 34, 38 provide the balanced input to amplifiers 54, 56 with microstrip output 40, 42 connecting the outputs of amplifiers 54, 56 to coplanar coupler 16 on the bottom surface. Coupler 16 has similar structure as coupler 14 with the U-shaped metal traces on the bottom surface connected to microstrip 40 and 42, and to output port 20 and isolation port 21 by conductive vias through the substrate.

In accordance with a feature of the invention, a bias voltage (at RF ground) can be connected by microstrip 44 on the top surface over and spaced from coupler 14 on the bottom surface, providing a bias voltage to circuitry shown generally at 50. The bias voltage line 44 is coupled to the ground layer on the bottom surface through capacitors 46 and vias 48. The cross-over structure allows DC bias to be taken at right angles to the coplanar coupler lines and cross over the coupler lines without degrading the performance of the

coplanar coupler while maintaining a high degree of electrical isolation between the coupler and the DC track. In another embodiment, the inverted coplanar coupler can have a center section under the DC bias cross-over which functions as a part grounded coplanar waveguide. By adjusting the amount of the grounded coplanar waveguide center section, the characteristics of the overall coupler can be optimized.

Fig. 3A illustrates the metal traces on a portion of the top surface of the substrate including input port and microstrip 10, isolation port and microstrip 11, amplifiers 54, 56, the output microstrip port 20 and output isolation port 21. Fig. 3B is a plan view of the bottom surface showing the metal layer 50 with a removed portion 24 in which is formed the coplanar coupler 14. Fig. 4 shows a three dimensional view of representative vias 48 and their role in interconnecting the top microstrip trace to the bottom coplanar waveguide traces. For example, these same improved coplanar couplers can be combined with mixers and modulators to form quadrature-balanced mixers and modulators. A single improved coplanar coupler can be applied in conjunction with an in-phase divider/combiner to form IQ modulators and image reject mixers.

There has been described an improved coplanar coupler for use with microstrip input and output lines in a quadrature power division and amplification application. While the invention has been described with reference to a specific embodiment, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1                   1.     In a microwave circuit having a coplanar coupler for microstrip input  
2 and output ports on a printed circuit substrate, the improvement comprising:

3                   a)     placing microstrip input and output lines on one surface of the  
4 substrate,  
5                   b)     placing coplanar coupler lines on another surface of the substrate, and  
6                   c)     interconnecting the microstrip input and output lines on the one surface  
7 to the coplanar coupler lines on another surface.

1                   2.     The improvement as defined by claim 1 wherein the step of c) includes  
2 the use of feedthrough vias.

1                   3.     The improvement as defined by claim 2 wherein the coplanar coupler  
2 lines comprise first and second metal lines in spaced-parallel alignment.

1                   4.     The improvement as defined by claim 3 wherein each of the first and  
2 second metal lines is U-shaped.

1                   5.     The improvement as defined by claim 4 and further including the step  
2 of:  
3                   d)     providing a bias voltage metal line on the one surface extending across  
4 and spaced from the first and second metal lines of the coplanar coupler.

1                   6.     The improvement as defined by claim 1 and further including the step  
2 of:  
3                   d)     providing a bias voltage metal line on the one surface extending across  
4 and spaced from the first and second metal lines of the coplanar coupler.

1                   7.     A coplanar coupler for use with microstrip input and output ports  
2 comprising:

3                   a)     a printed circuit substrate having top and bottom surfaces,  
4                   b)     first and second metal input ports formed on the top surface,  
5                   c)     first and second metal output ports formed on the top surface,

6 d) a metal layer on the bottom surface functioning as a ground plane for  
7 the input ports and the output ports as microstrip, the metal layer being removed in a coupler  
8 region under at least portions of the metal input and output ports and extending therebetween,

9 e) first and second metal lines on the bottom surface in the coupler region  
10 functioning as a coplanar coupler for the input port and output port, and

11 f) electrical connectors connecting one input port and one output port to  
12 the first metal line and connecting the other input port and the other output port to the second  
13 metal line.

1 8. The coplanar coupler as defined by claim 7 wherein the first and  
2 second metal lines are in spaced parallel arrangement.

1 9. The coplanar coupler as defined by claim 8 wherein each of the first  
2 and second metal lines is U-shaped.

1 10. The coplanar coupler as defined by claim 8 wherein the electrical  
2 connectors are feedthrough vias in the substrate.

1 11. The coplanar coupler as defined by claim 10 wherein the substrate is  
2 ceramic.

1 12. The coplanar coupler as defined by claim 11 wherein the metal is  
2 selected from the group consisting of gold, silver, and copper.

1 13. The coplanar coupler as defined by claim 12 and further including a  
2 bias voltage metal line on the top surface extending across and spaced from the first and  
3 second metal lines of the coplanar coupler.

1 14. The coplanar coupler as defined by claim 7 wherein the electrical  
2 connectors are feedthrough vias in the substrate.

1 15. The coplanar coupler as defined by claim 14 wherein the substrate is  
2 ceramic.

1 16. The coplanar coupler as defined by claim 15 wherein the metal is  
2 selected from the group consisting of gold, silver, and copper.

- 1           17.    The coplanar coupler as defined by claim 7 and further including a bias
- 2   voltage metal line on the top surface extending across and spaced from the first and second
- 3   metal lines of the coplanar coupler.



1/4

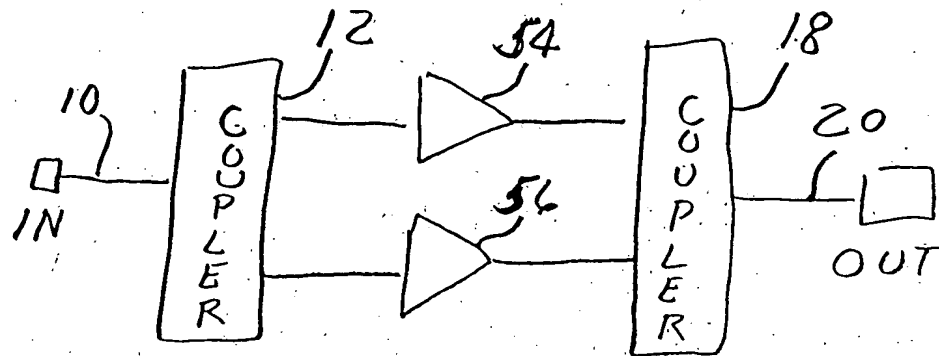


FIG. 1  
PRIOR ART

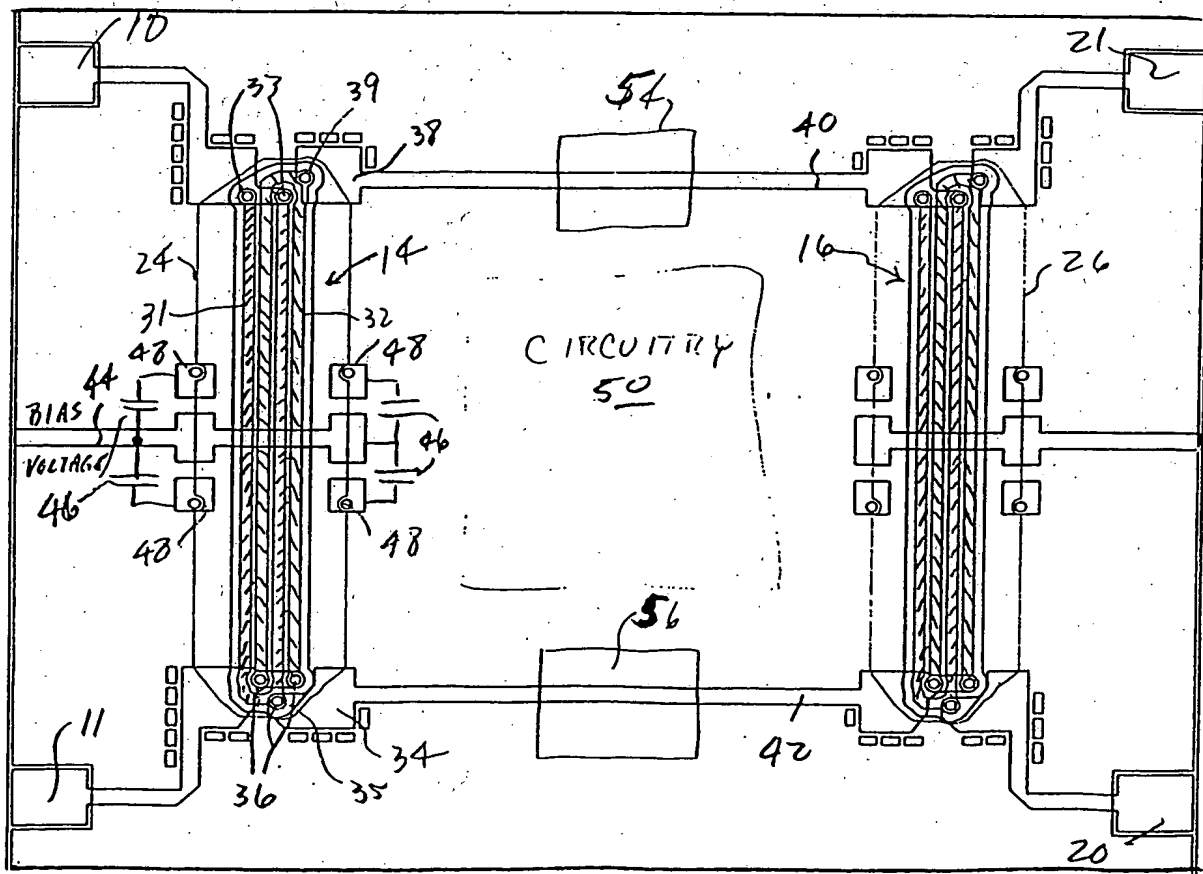
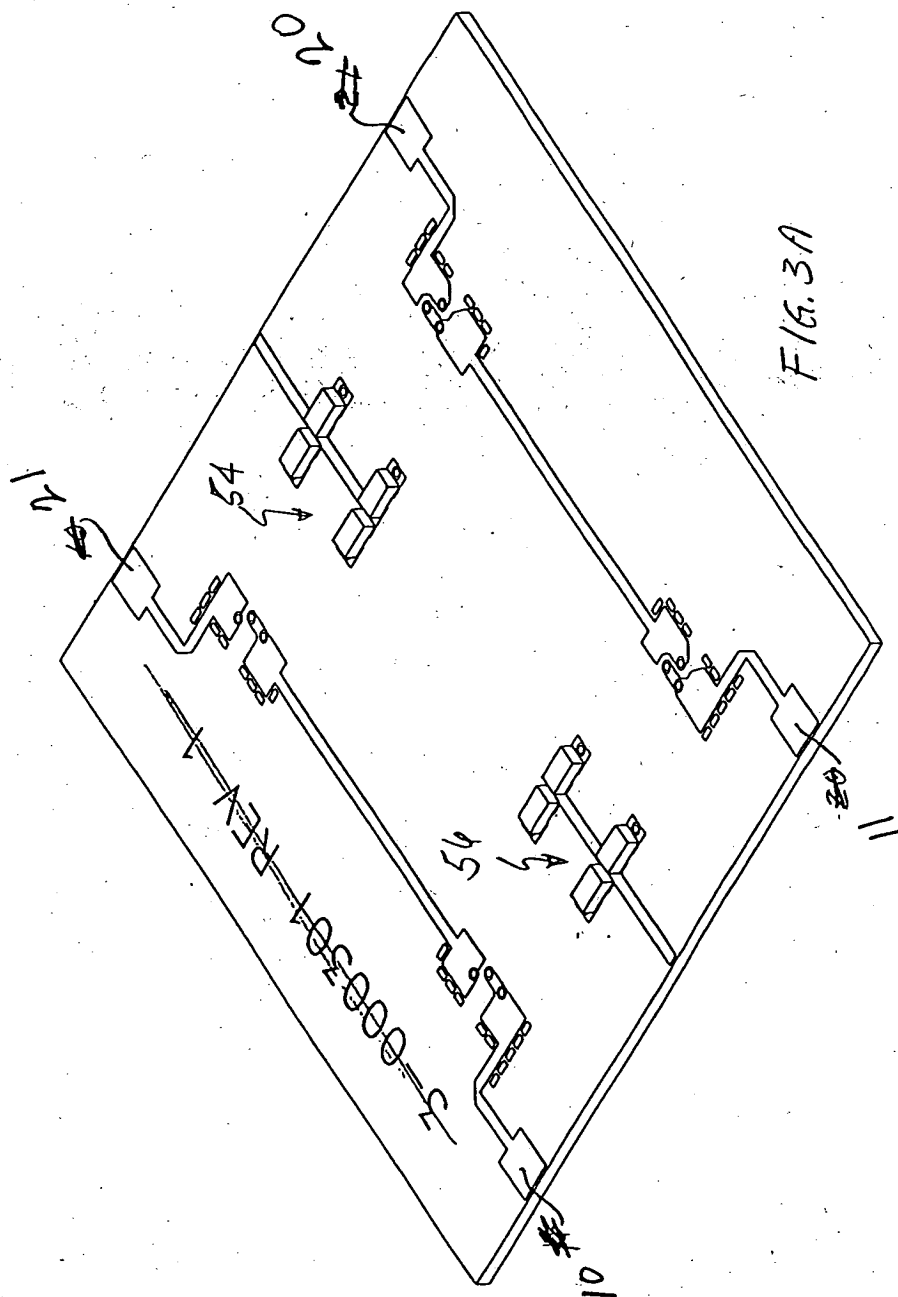


FIG. 2

2/4



3/4

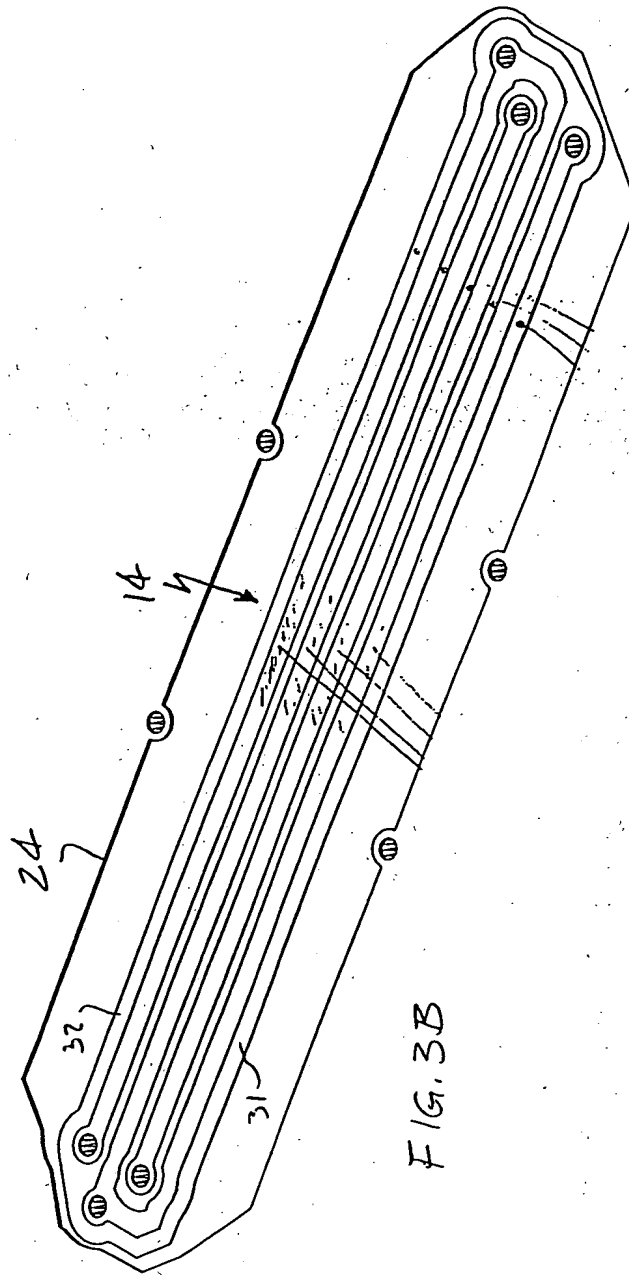
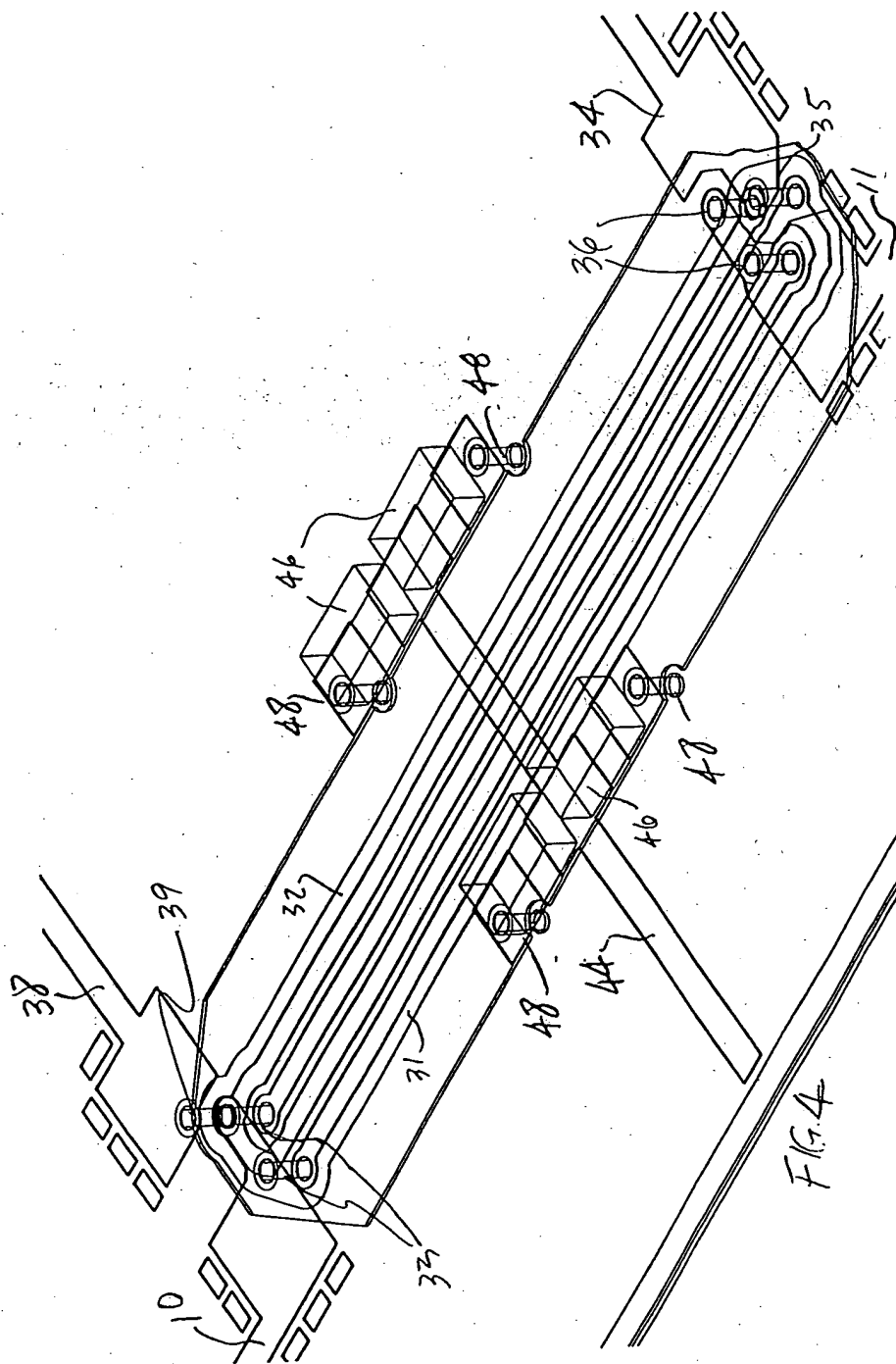


FIG. 3B



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US02/23045

**A. CLASSIFICATION OF SUBJECT MATTER**IPC(7) : H01P 5/18  
US CL : 333/116, 246

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**Minimum documentation searched (classification system followed by classification symbols)  
U.S. : 333/116, 246

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,446,425 A (BANBA) 29 August 1995 (29.08.1995), figures 1-4	1-4, 7-10 and 14
Y		11, 12, 15 and 16
A		5, 6, 13 and 17
Y	US 5,329,263 A (MINAMI) 12 July 1994 (12.07.1994), col. 2, lines 50-69	11, 12, 15 and 16

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.**\* Special categories of cited documents:**

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "B" earlier application or patent published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search

06 September 2002 (06.09.2002)

Name and mailing address of the ISA/US  
Commissioner of Patents and Trademarks  
Box PCT  
Washington, D.C. 20231  
Facsimile No. (703)305-3230

Date of mailing of the international search report

03 JAN 2003

Authorized officer

Dean O. Takaoka

Telephone No. (703) 305-6242

Deborah P. Vega  
Paralegal SpecialistTechnology Center 2800  
(703) 308-3078

**THIS PAGE BLANK (USPTO)**